What is claimed is:

1. A CMOS circuit comprising:

a first gate reference voltage

a first bias current source; and

a device having its gate coupled to the first gate reference voltage, the device coupled in series with the first bias current source and having a gate size and structure to enhance its sensitivity to process, voltage and temperature variations thereby compensating the first bias current source for same.

2. A CMOS circuit as claimed in Claim 1, wherein the size of the gate is a relatively short length.

3. A CMOS circuit as claimed in Claim 1, wherein the structure of the gate is a plurality of stripes.

4. A CMOS circuit as claimed in Claim 3, wherein the stripes are relatively short.

5. A CMOS circuit as claimed in Claim 1, further comprising a delay cell coupled between the first bias current and the device.

6. A CMOS circuit as claimed in Claim 1, further comprising a delay lock loop coupled between the first bias current and the device.

7. A CMOS circuit as claimed in Claim 1, further comprising a phase lock loop coupled between the first bias current and the device.

8. A CMOS circuit as claimed in Claim 1, further comprising an operational amplifier coupled between the first bias current and the device.

9. A CMOS circuit as claimed in Claim 1, further comprising an input/output pad coupled between the first bias current and the device.

10. A CMOS circuit as claimed in Claim 1, further comprising a charge pump coupled between the first bias current and the device.

11. A physical layer segment including:

a transmitter having:

an output coupled to a communication medium,

and a first pseudo-random bit-stream generator coupled to said output,

a receiver having:

an input coupled to a communication medium,

a second pseudo-random bit-stream generator

and a comparator coupled to said input and said second pseudo-random bit-stream generator;

12. A physical layer segment according to claim 11 wherein the receiver includes, a bit error rate counter coupled to said comparator.

13. A method of establishing data integrity comprising:

receiving a series of vectors,

generating the first of a series of pseudo-random vectors,

comparing said received and said first generated vector,

and after a positive comparison,

generating the remainder of said series and comparing these with subsequently received vectors.

14. A multiplexing circuit having:

a test data input;

a plurality of non-test data inputs;

an output;

a test mode selection input;

a selection input;

a plurality of intermediate signal lines;

an enabling means, coupled to said test mode selection input, for determining which of said plurality of non-test data inputs or said test data input is coupled said plurality of intermediate signal lines;

and a selection means, coupled to said selection input, for determining which of said intermediate signal lines is coupled to said output.

15. The multiplexing circuit according to claim 14 wherein a clock signal is coupled to the selection input.

16. The multiplexing circuit according to claim 15 wherein the output is coupled to a double data rate data signal.

17. The multiplexing circuit according to claim 14 wherein a JTAG test output data is coupled to the test data input and a JTAG test mode enable signal is coupled to the test mode selection input.

18. A physical layer segment including a delay line generator comprising:
A first bias generator,
And a second bias generator having:
a positive reference,
a negative reference,
a first bandgap reference,
and a second bandgap reference,
A voltage control input,
A delay line output,
A first MOSFET having a first doping,
Conductively coupling said first reference to said delay line output,
And coupled at its gate to said voltage control input,
A second MOSFET having a first doping,
Conductively coupling said first reference to said delay line output,
And coupled at its gate to said first bandgap reference,

A third MOSFET having a complementary doping to said first doping,

Conductively coupling said second reference to said delay line output,

And coupled at its gate to said second bandgap reference,

And a fourth MOSFET having a complementary doping to said first doping,

Conductively coupling said second reference to said delay line output,

And coupled at its gate to said delay line output.